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1 System level modeling and verification: Embedded systems verification with FGPA-enhanced in-circuit emulator
M. Meerwein, C. Baumgartner, T. Wieja, W. Glauert
September 2000 **Proceedings of the 13th international symposium on System synthesis ISSS '00**
Publisher: IEEE Computer Society
Full text available: pdf(109.43 KB) Additional Information: full citation, abstract, references, citings

In this paper we present a novel coverification concept for embedded microcontrollers that satisfies industrial requirements. Based on a commercially available CPU in-circuit emulator coupled with FPGA boards, it verifies the correctness of an implementation in terms of function and timing within a real-world environment.Using our system, the software engineer can write, test and optimize programs for a chip that is not yet physically existent. In addition the system is used to obtain software m ...

2 Verification of a Microcontroller IP Core for System-on-a-Chip Designs Using Low-Cost Prototyping Environments
Stephen Schmitt, Wolfgang Rosenstiel
February 2004 **Proceedings of the conference on Design, automation and test in Europe - Volume 3 DATE '04**
Publisher: IEEE Computer Society
Full text available: pdf(281.80 KB) Additional Information: full citation, abstract, index terms

Rapid prototyping is a fast and efficient way for the functional verification of Systems-on-a-Chip in an early stage of the design process. Because of the rising part of software in those systems the use and reuse of microcontroller IP cores is necessary to keep development cycles short. Today, prototyping of such IP cores is done with large and expensive hardware emulation machines consisting of many processor or FPGA-based prototyping boards. In this paper the authors describe an alternative p ...

3 Reusable embedded in-circuit emulator
Ing-Jer Huang, Hsin-Ming Chen, Chung-Fu Kao

January 2001 **Proceedings of the 2001 conference on Asia South Pacific design automation ASP-DAC '01**

Publisher: ACM Press

Full text available: pdf(88.97 KB) Additional Information: full citation, abstract, references, index terms

In this paper, we o introduce the Reusable Embedded In-Circuit Emulator (EICE) and Reusable EICE development system. The main function in EICE we design are testing and debugging. The architecture of EICE is reusable and based on IEEE 1149.1 boundary scan architecture. The EICE development system can help EICE to reduce developing time while developing a microcontroller/microprocessor. We implemented EICE by ASIC and FPGA way and the development system had been demonstrated in two microcont ...

4 Multi-processor operating system emulation framework with thermal feedback for systems-on-chip

Salvatore Carta, Andrea Acquaviva, Pablo G. Del Valle, David Atienza, Giovanni De Micheli, Fernando Rincon, Luca Benini, Jose M. Mendias

March 2007 **Proceedings of the 17th great lakes symposium on Great lakes symposium on VLSI GLSVLSI '07**

Publisher: ACM Press

Full text available: pdf(700.42 KB) Additional Information: full citation, abstract, references, index terms

Multi-Processor System-On-Chip (MPSoC) can provide the performance levels required by high-end embedded applications. However, they do so at the price of an increasing power density, which may lead to thermal runaway if coupled with low-cost packaging and cooling. Hence, mechanisms to efficiently evaluate the effectiveness of advanced thermal-aware operating-system (OS) strategies (e.g. task migration) onto the available MPSoC hardware are needed. In this paper, we propose a new MPSoC OS emulati ...

Keywords: FPGA, MPSoC, emulation, operating system, thermal studies

5 ICEBERG: an embedded in-circuit emulator synthesizer for microcontrollers

Ing-Jer Huang, Tai-An Lu

June 1999 **Proceedings of the 36th ACM/IEEE conference on Design automation DAC '99**

Publisher: ACM Press

Full text available: pdf(705.18 KB) Additional Information: full citation, references, citings, index terms

6 The case for a configure-and-execute paradigm

Frank Vahid, Tony Givargis

March 1999 **Proceedings of the seventh international workshop on Hardware/software codesign CODES '99**

Publisher: ACM Press

Full text available: pdf(484.64 KB) Additional Information: full citation, references, citings, index terms

Keywords: IP, cores, methodology, system-on-a-chip

7 Declic: Linux 2.6 on the international space station
Taco Walstra
August 2004 **Linux Journal**, Volume 2004 Issue 124
Publisher: Specialized Systems Consultants, Inc.
Full text available: html(21.76 KB) Additional Information: full citation, abstract

Linux fits into this new research program in several ways, from meeting real-time requirements with the 2.6 kernel to offering a prototyping platform for microcontroller code.

8 Fast development of source-level debugging system using hardware emulation (short paper)
Sang-Joon Nam, Jun-Hee Lee, Byoung-Woon Kim, Yeon-Ho Im, Young-Su Kwon, Kyong-Gu Kang, Chong-Min Kyung
January 2000 **Proceedings of the 2000 conference on Asia South Pacific design automation ASP-DAC '00**
Publisher: ACM Press
Full text available: pdf(204.60 KB) Additional Information: full citation, references

9 Experiences teaching an FPGA-based embedded systems class
Stephen A. Edwards
October 2005 **ACM SIGBED Review**, Volume 2 Issue 4
Publisher: ACM Press
Full text available: pdf(407.55 KB) Additional Information: full citation, abstract, references, index terms

I describe a two-year-old embedded systems design course I teach at Columbia University. In it, the students learn low-level C programming and VHDL coding to design and implement a project of their own choosing. The students implement their projects using Xilinx FPGAs and tools running on Linux workstations.The main challenges the students face are understanding and complying with complex and often poorly-documented interfaces and protocols, personal time management, and teamwork. While all real ...

10 Forth: Tina: an improbable 3-pin microcontroller
Paul Frenger
February 2005 **ACM SIGPLAN Notices**, Volume 40 Issue 2
Publisher: ACM Press
Full text available: pdf(550.74 KB) Additional Information: full citation, abstract, references, citings, index terms

The twenty-first century is rapidly becoming the age of nanotechnology. Everything seems to be getting smaller these days, especially in the electronic and scientific fields. The fuel-efficient Mazda Miata and Toyota MR2 have become the city commuter's must-have vehicles. The bulky boom-box has been replaced by the more socially responsible Apple iPod, with its miniscule rotating hard disk drive. The familiar 5-inch CD is being replaced by 3-inch versions, with smaller ones on the horizon. The p ...

11 Challenges in CAD for the one million gate FPGA
Kurt Keutzer
February 1997 **Proceedings of the 1997 ACM fifth international symposium on Field-programmable gate arrays FPGA '97**

Publisher: ACM Press
Full text available: pdf(389.50 KB) Additional Information: full citation, index terms

12 Reconfigurable computing: architectures and applications: Using reconfigurability to achieve real-time profiling for hardware/software codesign
Lesley Shannon, Paul Chow
February 2004 **Proceedings of the 2004 ACM/SIGDA 12th international symposium on Field programmable gate arrays FPGA '04**
Publisher: ACM Press
Full text available: pdf(228.02 KB) Additional Information: full citation, abstract, references, citings, index terms

Embedded systems combine a processor with dedicated logic to meet design specifications at a reasonable cost. The attempt to amalgamate two distinct design environments introduces many problems, one being how to partition a single design for the two platforms to achieve the best performance with the least effort. Since the latest FPGA technology allows the integration of soft or hard CPU cores with dedicated logic on a single chip, this presents new opportunities for addressing hardware/software ...

Keywords: FPGA, embedded processor, hardware/software codesign, performance measurement, profiling, soft processor

13 Linking codesign and reuse in embedded systems design
M. Meerwein, C. Baumgartner, W. Glauert
May 2000 **Proceedings of the eighth international workshop on Hardware/software codesign CODES '00**
Publisher: ACM Press
Full text available: pdf(77.16 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper presents a complete codesign environment for embedded systems which combines automatic partitioning with reuse from a module database. Special emphasis has been put on satisfying the requirements of industrial design practice and on the technical and economic constraints associated with automotive control applications. The object-oriented database architecture allows efficient management of a large number of modules. Experimental results from a real-world example demonstr ...

14 Special issue: dasCMP'05: A chip prototyping substrate: the flexible architecture for simulation and testing (FAST)
John D. Davis, Stephen E. Richardson, Charis Charitsis, Kunle Olukotun
November 2005 **ACM SIGARCH Computer Architecture News**, Volume 33 Issue 4
Publisher: ACM Press
Full text available: pdf(333.79 KB) Additional Information: full citation, abstract, references, index terms

We describe a hybrid hardware emulation environment: the Flexible Architecture for Simulation and Testing (FAST). FAST integrates field-programmable gate arrays (FPGAs), microprocessors, and memory to enable rapid prototyping of chip multiprocessors, multithreaded architectures, or other novel computer architectures and chip-level memory systems. FAST combines configurable and fixed-function hardware and software to facilitate rapid prototyping by utilizing components optimized for their particu ...

15 Verification techniques: Hardware-accelerated path-delay fault grading of functional test programs for processor-based systems

Paolo Bernardi, Michelangelo Grosso, Matteo Sonza Reorda

March 2007 **Proceedings of the 17th great lakes symposium on Great lakes symposium on VLSI GLSVLSI '07**

Publisher: ACM Press

Full text available: pdf(369.21 KB) Additional Information: full citation, abstract, references, index terms

The path-delay fault simulation of functional tests on complex circuits such as current processor-based systems is a daunting task. The amount of computing power and memory needed for verifying or grading functional test programs capabilities employing traditional techniques is huge and constitutes a serious bottleneck in the test flow. In this paper we propose a new mechanism for grading functional test program path-delay coverage (1) relying on FPGA-based emulation, (2) based on suitable instr ...

Keywords: FPGA, fault-emulation, path-delay, software-based testing

16 A decade of reconfigurable computing: a visionary retrospective

R. Hartenstein

March 2001 **Proceedings of the conference on Design, automation and test in Europe DATE '01**

Publisher: IEEE Press

Full text available: pdf(768.00 KB) Additional Information: full citation, references, citings, index terms

17 Instruction Set Emulation for Rapid Prototyping of SoCs

Jurgen Schnerr, Gunter Haug, Wolfgang Rosenstiel

March 2003 **Proceedings of the conference on Design, Automation and Test in Europe - Volume 1 DATE '03**

Publisher: IEEE Computer Society

Full text available: pdf(129.16 KB) Publisher Site Additional Information: full citation, abstract, index terms

In this paper the application of Instruction Set Emulation for rapid prototyping of SoCs will be presented. The emulation works in a way that both the software and the hardware behaviour of the emulated processor core is reproduced cycle accurately. This requires the use of hardware and software components. The hardware component consists of a board containing a VLIW processor and FPGAs. The software component is an instruction set simulator of the core running on the VLIW processor. The FPGAs a ...

18 Testbench, verification and debugging: practical considerations: Re-use-centric architecture for a fully accelerated testbench environment

Renate Henftling, Andreas Zinn, Matthias Bauer, Martin Zambaldi, Wolfgang Ecker

June 2003 **Proceedings of the 40th conference on Design automation DAC '03**

Publisher: ACM Press

Full text available: pdf(164.16 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper presents a new technology that accelerates functional system verification. Starting with a behavioral testbench, we developed a seamless flow to generate a re-use-oriented architecture for a synthesizable testbench without loosing compatibility towith the original testbench. Consequently, we combine the flexibility of a behavioral testbench and the simulation performance of a synthesizable testbench, while greatly reducing the modeling overhead.The approach itself is hardware independ ...

Keywords: acceleration, functional verification, hardware testbench

19 Cycle Accurate Binary Translation for Simulation Acceleration in Rapid Prototyping of SoCs

Jurgen Schnerr, Oliver Bringmann, Wolfgang Rosenstiel

March 2005 **Proceedings of the conference on Design, Automation and Test in Europe - Volume 2 DATE '05**

Publisher: IEEE Computer Society

Full text available: pdf(138.92 KB) Additional Information: full citation, abstract, index terms

In this paper, the application of a cycle accurate binary translator for rapid prototyping of SoCs will be presented. This translator generates code to run on a rapid prototyping system consisting of a VLIW processor and FPGAs. The generated code is annotated with information that triggers cycle generation for the hardware in parallel to the execution of the translated program. The VLIW processor executes the translated program whereas the FPGAs contain the hardware for the parallel cycle genera ...

20 Forth report: Ten years of Forth in ACM Sigplan Notices: part 1

Paul Frenger

November 2005 **ACM SIGPLAN Notices**, Volume 40 Issue 11

Publisher: ACM Press

Full text available: pdf(1.04 MB) Additional Information: full citation, abstract, references, index terms

So here we are: ten years of the *ACM Sigplan Notices Forth Report* is behind us. How amazing it is that we have reached this milestone! I hope that this column's longevity is a reflection of its popularity and perceived value to our readers.

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1 Fast power estimation for deterministic input streams

Luca Benini, Giovanni De Micheli, Enrico Macii, Massimo Poncino, Riccardo Scarsi

November 1997 **Proceedings of the 1997 IEEE/ACM international conference on Computer-aided design ICCAD '97**

Publisher: IEEE Computer Society

Full text available: pdf(958.88 KB) Publisher Site

Additional Information: full citation, abstract, references, citings, index terms

The power dissipated by digital systems under realistic input stimuli is not accurately described by a single average value, but by a waveform that shows how power consumption varies over time as the system responds to the inputs. We face the problem of obtaining accurate power waveforms for combinational and sequential circuits under typical usage patterns. We propose a multi level simulation engine that achieves high accuracy in estimating the average power as well as the time domain power wav ...

Keywords: accurate power waveforms, average power, combinational circuits, computational efficiency, deterministic input streams, digital systems, fast power estimation, multi level simulation engine, power consumption, power dissipation, realistic input stimuli, sequential circuits, time domain power waveform, typical usage patterns

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1 Implementation and emulation: An FPGA-based Pentium® in a complete desktop system

Shih-Lien L. Lu, Peter Yiannacouras, Rolf Kassa, Michael Konow, Taeweon Suh
February 2007 **Proceedings of the 2007 ACM/SIGDA 15th international symposium on Field programmable gate arrays FPGA '07**
Publisher: ACM Press
Full text available: pdf(195.80 KB) Additional Information: full citation, abstract, references, index terms

Software simulation has been the predominant method for architects to evaluate microprocessor research proposals. There are three tenets in modeling new designs with software models: simulation speed, model accuracy and model completeness. The increasing complexity of the processor and accelerated trend to have multiple processors on a chip are putting burden on simulators to achieve all tenets mentioned, including accurately capturing OS effects. In this work we perform preliminary experimentat ...

Keywords: FPGA, accelerator, emulator, pentium®, processor

2 An embedded DRAM architecture for large-scale spatial-lattice computations

Norman Margolus
May 2000 **ACM SIGARCH Computer Architecture News , Proceedings of the 27th annual international symposium on Computer architecture ISCA '00**, Volume 28 Issue 2
Publisher: ACM Press
Full text available: pdf(376.78 KB) Additional Information: full citation, abstract, references, citings, index terms

Spatial-lattice computations with finite-range interactions are an important class of easily parallelized computations. This class includes many simple and direct algorithms for physical simulation, virtual-reality simulation, agent-based modeling, logic simulation, 2D and 3D image processing and rendering, and other volumetric data processing tasks. The range of applicability of such algorithms is completely dependant upon the lattice-sizes and processing speeds that are computationally fe ...

Keywords: PIM, cellular automata, lattice gas, virtual processor

3 Special issue: dasCMP'05: Exploring the cache design space for large scale CMPs

Lisa Hsu, Ravi Iyer, Srihari Makineni, Steve Reinhardt, Donald Newell
November 2005 **ACM SIGARCH Computer Architecture News**, Volume 33 Issue 4

Publisher: ACM Press

Full text available: pdf(347.09 KB) Additional Information: full citation, abstract, references, index terms

With the advent of dual-core chips in the marketplace, small-scale CMP (chip multiprocessor) architectures are becoming commonplace. We expect a continuing trend of increasing the number of cores on a die to maximize the performance/power efficiency of a single chip. We believe an era of large-scale CMPs (LCMPs) with several tens to hundreds of cores is on the way, but as of now architects have little understanding of how best to build a cache hierarchy given such a large number of cores/threads ...

4 Optimizing 10-Gigabit Ethernet for Networks of Workstations, Clusters, and Grids: A Case Study

Wu-chun Feng, Justin (Gus) Hurwitz, Harvey Newman, Sylvain Ravot, R. Les Cottrell, Olivier Martin, Fabrizio Coccetti, Cheng Jin, Xiaoliang (David) Wei, Steven Low
November 2003 **Proceedings of the 2003 ACM/IEEE conference on Supercomputing SC '03**

Publisher: IEEE Computer Society

Full text available: pdf(209.19 KB) Additional Information: full citation, abstract, citings

This paper presents a case study of the 10-Gigabit Ethernet (10GbE) adapter from Intel R . Specifically, with appropriate optimizations to the configurations of the 10GbE adapter and TCP, we demonstrate that the 10GbE adapter can perform well in local-area, storage-area, system-area, and wide-area networks. For local-area, storage-area, and system-area networks in support of networks of workstations, network-attached storage, and clusters, respectively, we can achieve over 7-Gb/s end-to-end thro ...

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↑ ABSTRACT

In this paper, we o introduce the Reusable Embedded In-Circuit Emulator (EICE) and Reusable EICE development system. The main function in EICE we design are testing and debugging. The architecture of EICE is reusable and based on IEEE 1149.1 boundary scan architecture. The EICE development system can help EICE to reduce developing time while developing a microcontroller/microprocessor. We implemented EICE by ASIC and FPGA way and the development system had been demonstrated in two microcontroller.

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↑ Collaborative Colleagues:

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